What is claimed is:

1. An arithmetic unit comprising:

a memory for storing data;

an arithmetic logic unit for executing a predetermined arithmetic operation with respect to the data read from memory;

a register for temporarily storing the data read from the memory; and

a combining circuit for selecting one of the arithmetic logic unit and the register, and replacing a part of the data read from the memory with output data received from the selected one of the arithmetic logic unit and the register.

2. An arithmetic unit according to claim 1, wherein, when the part of the data read from the memory is replaced with an arithmetic result derived by the arithmetic logic unit, the combining circuit shifts the position of data to be replaced by a predetermined number of bits every time an operation process is executed.

3. An arithmetic unit according to claim 1, wherein the memory includes a plurality of memory blocks.

4. An arithmetic unit according to claim 1, wherein the arithmetic logic unit divide a carry signal in response to a division signal received thereto.

5. An arithmetic unit according to claim 1, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

6. An arithmetic unit according to claim 1, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.

7. An arithmetic unit comprising:

a memory for storing data;

an arithmetic logic unit capable of prohibiting ripple carry to an upper digit when a carry signal instructs a carry at an arbitrary bit position;

a register capable of storing data to be used in the arithmetic logic unit before an arithmetic operation is executed in the arithmetic logic unit; and

a combining circuit for selecting one of the arithmetic logic unit and the register, and replacing a part of the data read from memory with output data received from the selected one of the arithmetic logic unit and the register.

8. An arithmetic unit according to claim 7, wherein, when the part of the data read from the memory is replaced with an arithmetic result derived by the arithmetic logic unit, the combining circuit shifts the position of data to be replaced by a predetermined number of bits every time an operation process is executed.

9. An arithmetic unit according to claim 7, wherein the memory includes a plurality of memory blocks.

10. An arithmetic unit according to claim 7, wherein the arithmetic logic unit divide a carry signal in response to a

division signal received thereto.

11. An arithmetic unit according to claim 7, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

12. An arithmetic unit according to claim 7, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.

13. An arithmetic unit comprising:

a memory for storing a plurality of data in a successive manner; and

a combining circuit for inserting unused data after data of a predetermined combination to makeup a bit shortage for subsequent data of a predetermined combination to start from 0th or 8th bit when data of the predetermined combination is narrower in width than 2^n-bit.

14. An arithmetic unit according to claim 13, further comprising an arithmetic logic unit for executing a predetermined arithmetic operation with respect to the data read from memory.

15. An arithmetic unit according to claim 13, further comprising a register for temporarily storing the data read from the memory.

16. An arithmetic unit according to claim 14, wherein, when the part of the data read from the memory is replaced with an arithmetic result derived by the arithmetic logic unit, the combining circuit shifts the position of data to be replaced

by a predetermined number of bits every time an operation process is executed.

17. An arithmetic unit according to claim 13, wherein the memory includes a plurality of memory blocks.

18. An arithmetic unit according to claim 14, wherein the arithmetic logic unit divide a carry signal in response to a division signal received thereto.

19. An arithmetic unit according to claim 14, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

20. An arithmetic unit according to claim 14, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.